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## **METHODS AND ARRANGEMENTS FOR A LOW POWER PHASE- LOCKED LOOP**

### **ABSTRACT**

5               Methods and arrangements for a low power, phase-locked loop (PLL) are disclosed. Embodiments include a multi-phase oscillator like a voltage-controlled oscillator (VCO) to generate multiple phases of a clock signal. The multiple phases are then combined to generate a single clock signal having a frequency substantially equivalent to the number of phases multiplied by the frequency of the clock signal generated by the multi-phase VCO.

10   Advantageously, embodiments can generate clock signals having frequencies that are multiples of the frequency generated by the VCO, reducing the power consumed by the VCO to produce a clock signal having the same frequency as a clock signal generated by a single phase VCO. Further, the achievable frequency for the VCO is increased. In many embodiments, a high speed, n-bit frequency divider that implements a pulse latch facilitates the use of the multi-phase

15   VCO to generate the very high frequency clock signals.